REMARKS

This Amendment is filed along with a request for one month extension and appropriate fee in response to the Office Action dated July 27, 2007. Applicant first notes with appreciation the Examiner's thorough examination of the application as evidenced by the Office Action. In light of the Office Action, Applicant has amended claim 4 and has canceled claim 14. No new matter has been added by the amendment. Applicant respectfully submits that the claims are patentable over the cited references, and requests reconsideration and allowance of the claims in light of the following remarks.

Claim Rejections - 35 USC §112

Claim 14 currently stands rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement. Applicant has canceled claim 14, without prejudice. Accordingly, Applicant respectfully submits that the rejection of claim 14 is now moot.

Claim 4 is rejected due to an informality in relation to the recited range of claim 3, from which claim 4 depends. Applicant has amended claim 4 to recite a range that is consistent with respect to the range recited in claim 3. Accordingly, Applicant respectfully submits that the rejection of claim 4 is overcome. Applicant also respectfully submits that the amendment does not create new issues.

Claim Rejections - 35 USC §103

Claims 1-8 and 10 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Williams (U.S. Patent No. 6,291,298). Claims 12-19 are apparently also considered unpatentable over Williams although the Office Action is not explicit in this regard. Claims 9 and 11 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Williams in view of Jones (U.S. Patent No. 4,683,387). Applicant disagrees with these rejections.

The Office Action, in principle, refers to figure 7E of Williams in alleging that Williams anticipates independent claim 1. However, as previously pointed out by the Applicant, 7E figure

of Williams is not correct. Applicant has reproduced below figures 7E and 7F with Applicant's notes to illustrate inconsistencies in the Williams disclosure. As illustrated, the first part of the slope in figure 7E designated 10 is inversely proportional to an initial value of the input capacitance, that is $1/C_{iiss}$, during switching of the device. The second part 12 is inversely proportional to a final value during switching, which is $1/C_{fiss}$. The second part 12 is steeper than the first part 10, implying that $C_{fiss} < C_{iiss}$. This is unrealistic and is borne out by figure 7F, where it is clearly shown at 16 that the initial value C_{iiss} is smaller than a second effective value CG(eff) shown at 18. Essentially, the graph shows $1/C_{fiss} > 1/C_{iiss}$, which is $C_{fiss} < C_{iiss}$, which is not possible and wrong.

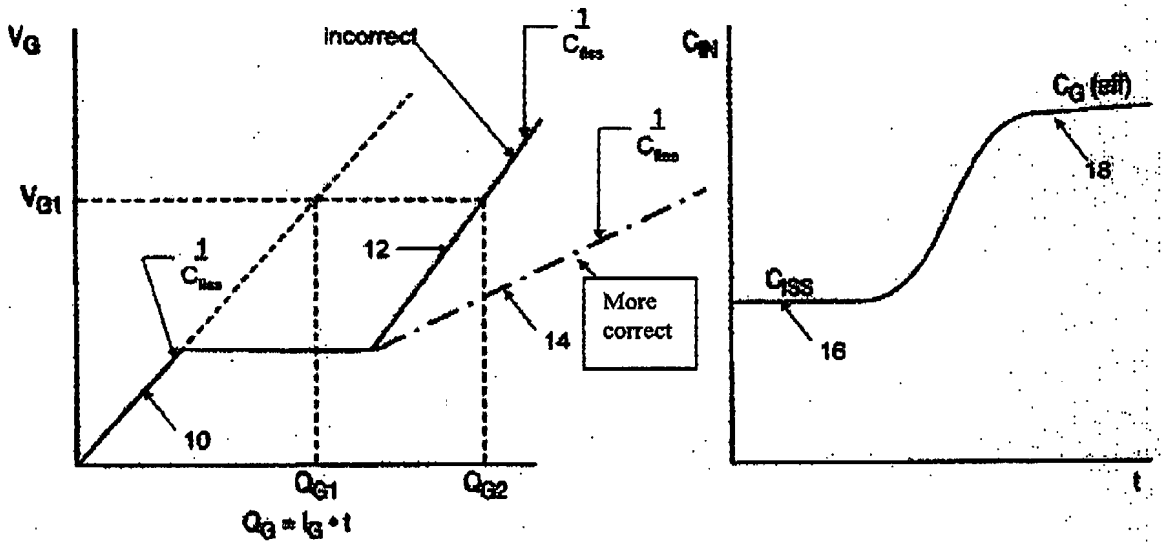

FIG. 7E FIG. 7F

See also the applicant's specification on page 1, line 16 to page 2, line 2, where it is stated:

> It is well known that the Miller effect has an influence on the input capacitance at the gate of devices of the aforementioned kind in that the input capacitance of a typical commercially available MOSFET varies during switching of the device.

> The input capacitance has a first value C_{iiss} when the device is off and a second value C_{fiss} when the device is on. The ratio of the second and first values for a known and commercially available IRF 740 power MOSFET is in the order of 2.5. It has been found that such a ratio impairs the switching speed of these devices.

The aforementioned second part of the slope after the Millar Plateau would have been more realistic, had it been shown as at 14 in the below reproduced figures.

Hence, in Fig 7E, Williams illustrates a situation wherein $C_{fiss}/C_{iiss} < 1.0$, which is unrealistic and wrong and, in any case, is not $1 < C_{fiss}/C_{iiss} < 2.0$ as recited in independent claim 1. The Office Action cites col. 4, lines 60-67 of Williams as indicating a ratio between the final value of capacitance when the device is on and the initial value of capacitance with the device is off as being smaller than 2.0. However, the cited passage includes no disclosure that can be fairly read to suggest such a ratio. Thus, Williams and more particularly the part relied on by the Office Action, does not teach the quantitative limitations cited in independent claim 1 as amended and accordingly does not anticipate or render obvious independent claim 1 as amended. In light of this, Applicant respectfully submits that independent claim 1, as well as the claims that depend therefrom, is patentable over the cited references.

Notably, the Office Action states that "differences in capacitance ratio will not support the patentability of subject matter encompassed by the prior art unless there is some evidence indicating such ratio are critical." In this regard, the Office Action cites *In re Aller* with respect to the proposition that, "Where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the workable ranges by routine experimentation". However, Applicant initially notes that Williams fails to set forth the general conditions of the claimed invention, specifically by virtue of Williams' failure to disclose the ratio of capacitance values set forth in the claimed invention, and also note that the ratio recited is critical.

In this regard, Williams relates to a process of manufacturing a trench gate semiconductor device having a gate oxide layer with multiple thicknesses. Referring to

figure 1, Williams discloses that the high electric field at the corner of the trench (106) during avalanche breakdown may be diminished by increasing the thickness of the gate oxide (110) at the bottom of the trench (see abstract). Hence, according to Williams, there is provided a device having a dielectric layer separating the gate electrode (104) from the semiconductor material (108) surrounding the trench in which the thickness of the dielectric layer is greater in a region at the bottom of the trench. This structure is aimed at reducing the strength of the electric field near the bottom of the trench, particularly the corner or rounded portion wherein the bottom of the trench makes a transition to a sidewall of the trench, and to reduce the capacitance (col. 5, line 66 to col. 6, line 8).

Meanwhile, the present application is directed to curing a noted deficiency of conventional MOSFET devices with respect to the slowness of switching (see page 1, line 10 to page 2, line 2 of the present application). In this regard, during switching of a conventional power MOSFET (e.g., such as the IRF 740) the ratio of the input capacitance of the device when it is on (C_{fiss}) and when the device is off (C_{iiss}) (i.e., C_{fiss}/C_{iiss}) is typically about 2.5, which impairs the switching speed of the device. Accordingly, the claimed invention is directed to providing a ratio of C_{fiss}/C_{iiss} at a lower ratio. Specifically, the claimed invention recites a range between about 1 and 2 for the ratio. Thus, the claimed ratio is critical to delivering the desired switching speed, as higher ratios will provide relatively low switching speeds.

Williams is directed to a conventional type MOSFET having a ratio of C_{fiss}/C_{iiss} that, based on the graph of figure 7F, appears to be about 2.25. Thus, Williams has not disclosed the general conditions of the claimed invention since the general conditions of the claimed invention require that the ratio of C_{fiss}/C_{iiss} is between 1 and 2. In fact, Williams in effect reduces the effect of drain to gate capacitance of the device only, but the feedback effect referred to in col. 4, lines 57-60 of Williams that impairs switching speed, is often dominated by the channel capacitance, which is not addressed by Williams. Furthermore, although Williams discloses thickening the oxide layer at the bottom of the trench only, in order to provide multiple thicknesses for the oxide later to overcome breakthrough problems, current practice is to have the oxide layer of the gate

as thin as possible to reduce the threshold voltage of the device. This also impairs the switching speed of the device. Thus, the disclosure of Williams not only fails to provide for a ratio of C_{fiss}/C_{iiss} that is below 2, but the disclosure of Williams is not suggestive of manipulations of the structure of a MOSFET that would provide such results. In fact, to the contrary, the feedback effect referred to in Williams at col. 4, lines 57-60 teaches away from the claimed invention since such feedback negatively impacts switching speed. However, in any case, the claimed ratio is critical to achieving increased switching speeds and thus, the ratio differentiates the claimed invention over Williams.

Furthermore, the ideal (but not practical) disclosure of the dashed line in figure 7E of Williams is not indicative of Williams disclosing a ratio of C_{fiss}/C_{iiss} that is below 2. To the contrary, as indicated above, the best ascertainable ratio of C_{fiss}/C_{iiss} that is determinable from the figures of Williams is about 2.25. Thus, since the claimed invention recites a ratio of C_{fiss}/C_{iiss} that is not disclosed or even contemplated by Williams, Williams cannot be fairly asserted to disclose the general conditions of the claimed invention. Moreover, the recitation of a ratio of C_{fiss}/C_{iiss} that is between 1 and 2 of independent claim 1 is not merely a workable range that is discoverable from Williams via routine experimentation since, as stated above, the state of the art would be to reduce the thickness of the oxide layer of the gate.

Finally, Applicant respectfully notes that paragraph 7 of page 4 of the final Office Action states that, with respect to the apparatus claimed in independent claim 1, the claims must be distinguished from the prior art in terms of structure rather than function. However, the cited paragraph apparently ignores the fact that independent claim 1 invokes 35 U.S.C. §112, sixth paragraph (see MPEP 2181). Accordingly, the function identified by the Office Action related to specifying the capacitance ratio "shall be construed to cover the corresponding structure ... described in the specification and equivalents thereof" (MPEP 2181 citing the patent laws).

Accordingly, for all the reasons stated above, Applicant respectfully submits that independent claim 1 and all the claims that depend therefrom are patentable over Williams for the reasons indicated above. Independent claims 15-18 include similar recitations to that of independent claim 1 with respect to the ratio of C_{fiss}/C_{iiss}.

Accordingly, independent claims 15-18 are patentable over Williams for the same reasons described above with regard to independent claim 1.

Jones fails to cure the deficiencies of Williams and is not cited as such. Accordingly, independent claim 1 is also patentable over the combination of Williams and Jones.

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CONCLUSION

In light of the amended and newly added claims and the remarks above, Applicant respectfully submits that the application is in condition for allowance and respectfully requests that a Notice of Allowance be issued. The Examiner is encouraged to contact Applicant's counsel to discuss any outstanding issues so as to expedite the application.

It is not believed that extensions of time or fees for net addition of claims are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 CFR § 1.136(a), and any fee required therefore (including fees for net addition of claims) is hereby authorized to be charged to Deposit Account No. 16-0605.

Respectfully submitted,

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